

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

0 250 171 B1

(17)

EUROPEAN PATENT SPECIFICATION

- (43) Date of publication of patent specification: 11.11.92 (51) Int. Cl.⁵: **H01L 21/82, H01L 27/15, H01L 27/06**
- (21) Application number: **87305209.6**
- (22) Date of filing: **12.06.87**

(54) **Compound semiconductor devices.**(30) Priority: **13.06.86 US 874295**(43) Date of publication of application:
23.12.87 Bulletin 87/52(45) Publication of the grant of the patent:
11.11.92 Bulletin 92/46(64) Designated Contracting States:
AT BE CH DE FR GB IT LI NL SE(56) References cited:
DE-A- 3 404 875

TECHNICAL DIGEST ON INTERNATIONAL ELECTRON DEVICES MEETING, Washington, DC, 1st-4th December 1985, pages 766-767; H.K. CHOI et al.: "Monolithic integration of Si MOSFETs and GaAs MESFETs"

TECHNICAL DIGEST ON GaAs IC SYMPOSIUM, Monterey, 12th-14th November 1985, pages 71-73, IEEE; R. FISCHER et al.: "Prospects for the monolithic integration of GaAs and Si"

Idem

IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 1, June 1979, page 401, New York, US; R. HUNG et al.: "Integrated light-emitting devices with silicon LSI circuits"

S.M. Sze, Ed, "VLSI Technology" (McGraw-Hill, Singapore 1983), pages 472-477, 502-503.

(73) Proprietor: **MASSACHUSETTS INSTITUTE OF TECHNOLOGY**
77 Massachusetts Avenue
Cambridge, MA 02139(US)

(72) Inventor: **Choi, Hong Kyun**
26 Phillip Farm Road
Concord Massachusetts 01742(US)
Inventor: **Tsaur, Bor-Yeu**
5 Richard Road
Bedford Massachusetts 01730(US)

(74) Representative: **Hughes, Brian Patrick et al**
Graham Watt & Co. Riverhead
Sevenoaks, Kent TN13 2BN(GB)

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid (Art. 99(1) European patent convention).

Description

Background Art

Monolithic integration of compound semiconductor (Group III-V or II-VI) devices and silicon devices on a common substrate has the potential for achieving very substantial improvements in the performance of Very Large Scale Integrated (VLSI) circuits. In particular, Monolithic integration of a GaAs compound semiconductor device and Silicon devices on a common substrate (MGS) enhances the VLSI circuit by combining the performance of silicon circuits with gallium arsenide and/or aluminum gallium arsenide optoelectronic components and high speed gallium arsenide and/or aluminum gallium arsenide circuits.

For example, the through-put of a silicon VLSI system may be considerably increased by integrating high-speed gallium arsenide input and/or output circuits, signal processing units and/or cache memory devices. As another example, gallium arsenide/aluminum gallium arsenide optoelectronic interface units may provide high-data-rate optical links to replace wire interconnects between silicon VLSI subsystems.

While there exists a 4% lattice mismatch between gallium arsenide and silicon; device-quality gallium arsenide layers have been grown on silicon substrates by both molecular beam epitaxy (MBE) and metal organic chemical vapor deposition. For true MGS integration, however, it is necessary to fabricate both gallium arsenide and silicon devices on the same wafer or substrate. Monolithic integration of GaAs and Si FET devices is known from Technical Digest on GaAs IC Symposium, Monterey, 12-14 November 1985, pages 71-73; and from Technical Digest on International Electron Devices Meeting, Washington, DC, 1-4 December 1985, pages 766-767. Integration of GaP and Si devices on a common Si substrate is also known from DE-A-3 404 875.

Disclosure of the Invention

The present invention relates, in general, to a method for fabricating compound semiconductor devices of III-V or II-VI material and semiconductor devices of silicon on a common substrate. The III-V material is preferably gallium arsenide or alloys of gallium arsenides, such as aluminum gallium arsenide. The II-VI material may comprise cadmium telluride. For ease in description, it should be understood that references hereafter to gallium arsenide are intended to also encompass aluminum gallium arsenide or other gallium arsenide metal alloys, as well as gallium arsenide itself, unless otherwise indicated.

The present invention is a method of fabricating compound semiconductor devices (210) of III-V or II-VI material and semiconductor devices (200) of silicon on a common substrate of a first conductivity type with low resistance interconnections between the compound semiconductor devices and the silicon devices formed in the substrate comprising the steps of:

(a) forming Si devices (200) having regions of a second conductivity type opposite to said first conductivity type (34'/30'/32') and wherein one of said regions (32') extends laterally along the planar surface of the substrate;

(b) forming a protective layer (16'/17') over the Si devices and the remainder of said substrate surface;

(c) forming openings laterally displaced from the Si devices through said protective layer to expose regions of the surface of said substrate, a portion of the perimeter of one of said openings being coextensive with said extended region, the substrate region underlying said opening being heavily doped to form a low resistance region (50) of said second conductivity type extending to the planar surface of the substrate in contact with the extended region;

(d) forming a layer (54) of said compound semiconductor on the protective layer and the exposed surface regions, which layer is single crystalline above the exposed surface regions and polycrystalline elsewhere;

(e) removing the compound semiconductor polycrystalline layer;

(f) forming said compound semiconductor devices (56/58/60/62) having junctions formed of second conductivity type regions on the remaining single crystalline compound semiconductor (54) with the low resistance region (50) contacting said extended region 32' of said Si devices to form said low resistance interconnection in said substrate; and

(g) forming ohmic contacts (72, 70, 28') on said devices (200, 210).

The foregoing and other features and advantages of the invention will now be described in connection with the drawings. It should be noted that in the embodiments shown herein, GaAs or AlGaAs has been chosen to illustrate the process, but as mentioned above, other III-V compounds or alloys, such as InP, etc., may be substituted therefore or II-VI compounds, such as CdTe may be employed in place of the III-V compounds.

Brief Description of the Drawings

Fig. 1A-D are schematic cross-sectional drawings of the silicon processing for an MGS, not forming part of the present invention, wherein a

silicon MOSFET is fabricated along with a gallium arsenide MESFET on a single silicon substrate.

Fig. 1A shows the silicon MOSFETs fabricated in selected areas of the silicon substrate and the device is covered with a protective layer of $\text{SiO}_2/\text{Si}_3\text{N}_4$.

Fig. 1B shows the gallium arsenide epitaxy processing step.

Fig. 1C shows the gallium arsenide MESFET processing, and

Fig. 1D shows the silicon contact formation and metallization process steps.

Fig. 2 is a plot of the transistor characteristics (current in milliamps v. voltage with 200 millivolt gate voltage steps between curves) of a gallium arsenide MESFET made in accordance with the invention.

Fig. 3 is a plot of the gate Schottky diode characteristics of a gallium arsenide MESFET made in accordance with the invention.

Fig. 4 is a plot of the silicon MOSFET characteristics (A) with and (B) without gallium arsenide MESFET processing steps.

Fig. 5 is a schematic cross-sectional diagram of a monolithically integrated silicon MOSFET 200 and gallium arsenide/aluminum gallium arsenide light emitting diode 210 made in accordance with the invention.

Fig. 6 is a drawing of a planar top view of the gallium arsenide/aluminum gallium arsenide LED 210 and the surrounding silicon MOSFET 200 of Fig. 5.

Fig. 7 is a plot of the silicon MOSFET characteristics of Figs. 5 and 6 (A) with and (B) without gallium arsenide/aluminum gallium arsenide LED processing steps.

Fig. 8 is a plot of the current vs. voltage characteristics of the MGS LED of Figs. 5 and 6.

Fig. 9 is a plot of a light output vs. current characteristics of the MGS LED of Fig. 5.

Fig. 10 is a plot of the modulation characteristics of an MGS LED at (A) 20 megahertz and (B) 27 megabits per second. The bottom, middle and top traces are the time wave forms of the gate voltage V_g , drain or LED current I , and light output L , respectively.

Best Mode of Carrying Out the Invention

I. INTEGRATION OF Si MOSFETs and GaAs MESFETs

The sequence of processing steps for fabricating MGS Si MOSFETs and GaAs MESFETs on an Si substrate is shown in Figs. 1A-D. This process has previously been published in Technical Digest on International Electron Devices Meeting, Wash-

ington, DC, 1-4 December 1985, pages 766-767. Referring to Fig. 1A, the Si MOSFETs 10 are fabricated first, except for contact openings and final metallization, on selected areas of a 1-3 ohm-cm p-type Si single crystal wafer or substrate 12 oriented 3° off the (100) crystallographic plane toward the (111) plane. A standard poly-Si gate process is used for MOSFET fabrication. This poly-Si process consists, in general, of forming a thermal oxide SiO_2 layer 14 over the wafer 12; forming openings through layer 14; forming a thin gate oxide layer 15; depositing a poly-Si layer (not shown) over the entire wafer; etching the poly-Si layer outside the gate area 30; performing ion implantation using poly-Si gate 30 and SiO_2 14/15 as a mask for ion implantation of drain and source n^+ regions 34 and 32, respectively. The gate region 30 is also doped by ion implantation at the same time to form an n^+ gate.

Chemical vapor deposition is then employed to cover the entire wafer with successive layers of SiO_2 16 and Si_3N_4 17 to protect the MOSFET structures during subsequent GaAs epitaxy and subsequent MESFET processing. The Si_3N_4 layer is used because SiO_2 is a poor diffusion barrier for Ga. However, for thin film, low temperature GaAs layers, a single layer of SiO_2 may be adequate.

Referring to Fig. 1B, 300×10^{-3} mm (300 micron) square openings are etched in the $\text{Si}_3\text{N}_4/\text{SiO}_2$ cap layers 17/16 and oxide layers 14/15 to expose the bare Si substrate surface in the regions where GaAs devices are to be fabricated. GaAs layers 18 are then grown over the entire wafer, such as by MBE.

Preferably, before being loaded into the MBE system, the wafer, as thus far processed, is thoroughly cleaned and any surface oxide present is etched from the bare Si regions by dipping in HF. The wafer is heated *in situ* to about 850°C for a short period to desorb any remaining surface oxide. GaAs growth is initiated at a relatively low temperature to promote GaAs nucleation, and the temperature is then raised to about 580°C for the remaining growth. The GaAs 20 grown on the bare surface Si 12 is single-crystal material, while that on the nitride 17 is polycrystalline 21.

Transmission electron microscopy shows that the single-crystal GaAs near the GaAs/Si interface has a dislocation density exceeding 10^{10} cm^{-2} due to the lattice mismatch. As growth continues, however, only a small fraction of the dislocations propagate toward the surface. Material with a dislocation density of $10^6 - 10^7 \text{ cm}^{-2}$ is obtained when the thickness exceeds about $2 \times 10^{-3} \text{ mm}$ (2 microns).

Referring to Fig. 1C, the GaAs layers grown for the MESFET structure 100 are a $4 \times 10^{-3} \text{ mm}$ (4 micron) thick nominally undoped buffer layer 20', an n active layer 22 doped with Si to 3×10^{17}

cm^{-3} , and an n+ contact layer 24 doped to more than $2 \times 10^{18} \text{ cm}^{-3}$.

The polycrystalline GaAs 21 is then etched away (as shown in Fig. 1C), and MESFETs are fabricated in the single-crystal regions by the conventional recessed gate process. The gate metal 27 is Al, and Ge/Au/Ni is used for ohmic contacts 26. Next, (See Fig. 1D) contact openings for the Si MOSFETs 10 are etched in the $\text{Si}_3\text{N}_4/\text{SiO}_2$ layers 17/16 and oxide layer 15, and metallization 28 to provide ohmic contacts is performed by evaporating Al to complete fabrication of MOSFET 10. Metal interconnections 29 may be similarly formed between the MESFET and MOSFET contacts.

An Si MOSFET with an adjacent GaAs MESFET has been fabricated, as above, in which the gate lengths of the Si and GaAs devices are 5 and 1 microns, respectively, and in which the gate width is 40 microns for both devices. The GaAs MESFETs have well behaved characteristics, as shown in the transistor I-V plot of Fig. 2, with transconductance of about 150 mS/mm. The measured source resistance is about 1 ohm-mm giving an intrinsic transconductance of about 175 mS/mm. The output conductance has a fairly low value of about 3.5 mS/mm. The gate Schottky diodes have a breakdown voltage of more than 10 V and negligible leakage current, as shown in Fig. 3, and the breakdown is sharp. These results are comparable to those obtained for state-of-the-art GaAs MESFETs of similar gate length fabricated on single-crystal GaAs substrates.

The MGS Si MOSFETs have normal transistor characteristics, as shown in Fig. 4A. The transconductance is about 19 mS/mm for a gate oxide thickness of 80 nm (800 Å). Fig. 4B shows the transistor characteristics of control devices fabricated on a separate Si wafer. The characteristics of the devices fabricated with and without GaAs processing steps are seen to be nearly identical.

II. INTEGRATION of Si MOSFETs AND GaAs/AlGaAs DOUBLE-HETEROSTRUCTURE LEDs

Fig. 5 is a partial schematic diagram of an embodiment of the invention in cross-section. In this embodiment GaAs/AlGaAs double-heterostructure, LEDs 210 are formed on a Si substrate 12' surrounded by a ring-type MOSFET 200. The right side of the ring is not shown in Fig. 5 for simplicity. The sequence of processing steps is as follows. After initial thermal oxidation 14' of a p-type Si wafer 12', openings of $200 \times 10^{-3} \text{ mm}$ (200 microns) \times $400 \times 10^{-3} \text{ mm}$ (400 microns) are etched in the SiO_2 14', and a high dose of arsenic ions is implanted to form n+ islands 50 by converting the surface of the exposed Si wafer 12'. A

Si MOSFET 200 is fabricated around each n+ island, except for contact openings and final metallization. The MOSFET drain region 32' is in contact with the edge of n+ island 50. The entire wafer is capped with successive layers of SiO_2 16' and Si_3N_4 17', and openings are etched to expose the n+ Si islands 50. It should be noted that the n+ Si islands 50 could be formed during the formation of the GaAs layer. Molecular beam epitaxy is employed to deposit the following series of layers for the LEDs: $3 \times 10^{-3} \text{ mm}$ (3 microns) thick n+ GaAs buffer 54, a $0.5 \times 10^{-3} \text{ mm}$ (0.5 microns) thick n $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ 56, a $0.4 \times 10^{-3} \text{ mm}$ (0.4 microns) thick p GaAs active 58, $0.5 \times 10^{-3} \text{ mm}$ (0.5 microns) thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ 60, and $0.25 \times 10^{-3} \text{ mm}$ (0.25 microns) thick p+ GaAs cap 62. The growth conditions are similar to those described in the previous embodiment above, except that the AlGaAs growth temperature is about 700°C .

The heavily doped n+ Si island 50 forms an internal low resistance interconnect between the drain 32' of the Si MOSFET 200 and the n+ GaAs cathode 54 of LED 210.

The polycrystalline GaAs/AlGaAs layers deposited as above on the $\text{Si}_3\text{N}_4/\text{SiO}_2$ cap are removed by etching. Octagonal mesas for LEDs are formed in the monocrystalline GaAs/AlGaAs islands grown on bare Si by etching down to the n+ GaAs buffer. Plasma-enhanced chemical vapor deposition is used to deposit SiN_x 64 over the entire wafer. Contact openings are etched in the nitride layer 64 for LEDs and in the nitride/oxide layer 64/17'/16' 15' 14' for MOSFETs. Metallization is performed by evaporating Al 28' on the MOSFETs and Ni/Ge/Au 70 and Cr/Au 72, respectively, on the cathode 54 and anode 62 of the LEDs 210.

Contact 28' to the MOSFET drain 32' and contact 70 to the LED cathode 54, although not utilized in joint operation of the two devices, are made in order to permit the characteristics of each device to be measured separately. To accommodate these additional contacts, it is necessary to increase the area of the n+ Si layer, thereby substantially increasing the drain/cathode capacitance.

Fig. 6 is a top planar view showing a completed GaAs/AlGaAs LED 210 surrounded by a Si MOSFET 200 made as described above. The LED mesa has a diameter of $75 \times 10^{-3} \text{ mm}$ (75 microns), and the unmetallized opening 80 for LED emission has a diameter of $50 \times 10^{-3} \text{ mm}$ (50 microns). The MOSFET has a gate length of $5 \times 10^{-3} \text{ mm}$ (5 microns) and gate width of 1.6 mm. The MGS MOSFETs 200 have normal transistor characteristics. Fig. 7A shows the characteristics of a typical device, which delivers about 120 mA with both gate and drain set at 5 V. Fig. 7B shows the characteristics of a control MOSFET fabricated on

a separate Si wafer. The characteristics of the devices fabricated with and without GaAs/AlGaAs growth and processing steps are seen to be almost the same.

The MGS LED 210 has a breakdown voltage of about 16 V with negligible leakage current, as shown in Fig. 8. This is the same as the value obtained for control devices fabricated on a GaAs substrate.

At low forward bias voltages, both the MGS and control LEDs have an ideality factor close to 2, indicating that recombination is the dominant mechanism of current flow. However, at a given bias voltage, the current is about 50 times higher for the MGS devices than for the control devices. This implies that the minority carrier lifetime is much shorter for the MGS GaAs/AlGaAs layers than for the control layers.

Fig. 9 shows the light output vs DC current characteristic for MGS LED 210. A microscope lens with numerical aperture of 0.65 was used to focus the light on a 1-cm-diameter p-i-n photodiode detector. The characteristic is slightly sublinear because of heating. At 100 mA DC current, the output is about 6.5 μ W, which is 10-15% of the output from control devices.

The MGS LEDs have a non-uniform near-field pattern with many dark spots, while the pattern for the control LEDs is uniform. The peak of the MGS LED spectrum is at 875 nm, about 5 nm greater than that for the control devices. The shift can be attributed to tensile stress in the MGS GaAs/AlGaAs layers.

To characterize the heterojunction between the n+ Si and n+ GaAs layers, an I-V curve was measured for current flow between the MOSFET drain and LED cathode contacts 28' and 70. The characteristic was ohmic, showing that there is no barrier to the heterojunction. The measured resistance was 3 ohms. This value represents an upper limit on the heterojunction resistance, since it includes the resistance of the drain and cathode contacts.

With the MGS LED anode 62 biased at 5 V, the light output was modulated by applying a stream of voltage pulses to the MOSFET gate 30'. The light was focused with the microscope lens on a 0.5-mm-diameter avalanche photodiode detector.

Fig. 10A shows the gate voltage, LED current, and light output waveforms obtained when the voltage pulses were applied at a repetition rate of 20 MHz. The current waveform is distorted with respect to the voltage waveform in a manner characteristic of charging and discharging a capacitance, but the light output closely follows the current. These observations show that the output modulation is limited not by the speed of the LED but by the rate at which the MOSFET charges and

discharges the drain/cathode capacitance, which is estimated to be about 200 pF. This conclusion is confirmed by the fact that modulation rates exceeding 100 MHz were obtained when the LED was driven directly with a pulse generator. Fig. 10B shows the waveforms obtained when a bit pattern was applied to the gate at a modulation rate of 27 Mbps. Although there is some pattern effect, each bit is clearly resolved.

III. SUMMARY

The monolithic integration of Si MOSFETs with GaAs MESFETs and also with GaAs/AlGaAs double-heterostructure LEDs, has been described. The operating characteristics of the MGS MOSFETs and MESFETs are comparable to those of similar devices fabricated on separate Si and GaAs substrates. LED modulation rates up to 27 Mbps have been accomplished by applying a stream of voltage pulses to the MOSFET gate. It should be possible to achieve much higher modulation rates by scaling down the device dimensions to reduce parasitic capacitance.

Equivalents

While the above described embodiments of the invention are preferred, other configurations will be readily apparent to those skilled in the art. For example, the term Si substrate or wafer is intended to include an SOS (Silicon on Sapphire) substrate, or a Silicon on Insulator (Si on SiO₂ on Si) substrate. In addition to LEDs, other optoelectronic devices may be fabricated on the exposed Si surface, such as lasers or light detectors. Other type transistors, such as bipolar or modulation doped FETs (MODFETs) may be substituted for the MESFETs or the Si MOSFETs.

Claims

1. A method of fabricating compound semiconductor devices (210) of III-V or II-VI material and semiconductor devices (200) of silicon on a common substrate of a first conductivity type with low resistance interconnections between the compound semiconductor devices and the silicon devices formed in the substrate comprising the steps of:

(a) forming Si devices (200) having regions of a second conductivity type opposite to said first conductivity type (34'/30'/32') and wherein one of said regions (32') extends laterally along the planar surface of the substrate;

(b) forming a protective layer (16'/17') over the Si devices and the remainder of said

substrate surface;

(c) forming openings laterally displaced from the Si devices through said protective layer to expose regions of the surface of said substrate, a portion of the perimeter of one of said openings being coextensive with said extended region, the substrate region underlying said opening being heavily doped to form a low resistance region (50) of said second conductivity type extending to the planar surface of the substrate in contact with the extended region;

(d) forming a layer (54) of said compound semiconductor on the protective layer and the exposed surface regions, which layer is single crystalline above the exposed surface regions and polycrystalline elsewhere;

(e) removing the compound semiconductor polycrystalline layer;

(f) forming said compound semiconductor devices (56/58/60/62) having junctions formed of second conductivity type regions on the remaining single crystalline compound semiconductor (54) with the low resistance region (50) contacting said extended region 32' of said Si devices to form said low resistance interconnection in said substrate; and

(g) forming ohmic contacts (72, 70, 28') on said devices (200, 210).

2. A method as claimed in claim 1, characterised in that the low resistance region (50) is formed before the protective layer (16'/17') is formed.
3. A method as claimed in claim 1, characterised in that the low resistance region is formed during the formation of the compound semiconductor layer.
4. A method as claimed in any preceding claim, characterised in that the substrate comprises a single crystal: silicon, or a silicon on sapphire, or a silicon-on-insulator substrate.
5. A method as claimed in any preceding claim, characterised in that the protective layer comprises a layer of SiO₂ (16').
6. A method as claimed in any preceding claim, characterised in that the protective layer comprises layers of SiO₂ (16') and Si₃N₄ (17').
7. A method as claimed in any preceding claim, characterised in that the compound semiconductor is GaAs or an alloy thereof.
8. A method as claimed in claim 7, characterised

in that the gallium arsenide semiconductor device is an optoelectronic device (210).

9. A method as claimed in any preceding claim, characterised in that the Si devices are part of an Si circuit.
10. A method as claimed in any preceding claim, characterised in that the compound semiconductor devices are transistors from the class comprising MESFETs, bipolar transistors, or modulation doped FETs.
11. A method as claimed in any preceding claim, characterised in that the compound semiconductor devices are optoelectronic devices from the class comprising LED, lasers and light detectors.
12. A method as claimed in any preceding claim, characterised in that the compound semiconductor devices are part of a circuit consisting of transistors and optoelectronic devices.
13. A method as claimed in any preceding claim, characterised in that the ohmic contacts for said Si devices and compound semiconductor devices is formed after the compound semiconductor device is formed and the ohmic contacts for the Si devices is formed through openings made in said protective layer.

Patentansprüche

1. Verfahren zum Herstellen von zusammengesetzten Halbleiteranordnungen (210) aus III-V- oder II-VI-Material und Halbleiteranordnungen (200) aus Silizium auf einem gemeinsamen Substrat eines ersten Leitfähigkeitstyps mit Verbindungen mit geringem Widerstand zwischen den zusammengesetzten Halbleiteranordnungen und den Siliziumanordnungen, die in dem Substrat gebildet sind, bestehend aus den Schritten, daß
 - a) Si-Anordnungen (200) mit Zonen eines zweiten Leitfähigkeitstyps gegenüber dem ersten Leitfähigkeitstyp (34'/30'/32') gebildet werden, wobei eine der Zonen (32') seitlich entlang der ebenen Oberfläche des Substrats fortgeführt ist,
 - b) eine Schutzschicht (16'/17') über den Si-Anordnungen und dem verbleibenden Teil der Substratoberfläche gebildet wird,
 - c) Öffnungen seitlich versetzt von den Si-Anordnungen durch die Schutzschicht hindurch gebildet werden, um Zonen der Oberfläche des Substrats freizulegen, wobei ein Bereich des Umfangs einer der Öffnungen

- die gleiche Erstreckung mit der fortgeführten Zone aufweist und die unter der Öffnung liegende Substratzone hochdotiert ist, um eine Zone (50) geringen Widerstands des zweiten Leitfähigkeitstyps zu bilden, die sich zur ebenen Oberfläche des Substrats in Kontakt mit der fortgeführten Zone erstreckt,
- d) eine Schicht (54) des zusammengesetzten Halbleiters auf der Schutzschicht und den freigelegten Oberflächenzonen gebildet wird, welche Schicht über den freigelegten Oberflächenzonen einkristallin und im übrigen polykristallin ist,
- e) die zusammengesetzte Halbleiter-Polykristallinschicht entfernt wird,
- f) die zusammengesetzten Halbleiteranordnungen (56/58/60/62) mit Übergängen gebildet werden, die von Zonen des zweiten Leitfähigkeitstyps auf dem verbleibenden einkristallinen zusammengesetzten Halbleiter (54) gebildet sind, wobei die Zone (50) geringen Widerstands die fortgeführte Zone (32') der Si-Anordnungen zur Bildung der Verbindung mit geringem Widerstand im Substrat berührt, und
- g) ohmsche Kontakte (72,70,28') auf den Anordnungen (200,210) gebildet werden.
2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Zone (50) mit niedrigem Widerstand gebildet wird, bevor die Schutzschicht (16',17') gebildet wird.
 3. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Zone mit niedrigem Widerstand während der Bildung der zusammengesetzten Halbleiterschicht gebildet wird.
 4. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß das Substrat ein Einkristall: Silizium oder ein Silizium auf Saphir oder ein Silizium-auf-Isolator-Substrat umfaßt.
 5. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die Schutzschicht eine Schicht aus SiO_2 (16') umfaßt.
 6. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die Schutzschicht Schichten aus SiO_2 (16') und Si_3N_4 (17') umfaßt.
 7. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß der zusammengesetzte Halbleiter GaAs oder eine Legierung von diesem ist.
 8. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß die Galliumarsenid-Halbleiteranordnung eine optoelektronische Anordnung (210) ist.
 9. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die Si-Anordnungen Teil eines Silizium-Schaltkreises sind.
 10. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die zusammengesetzten Halbleiteranordnungen Transistoren der Klasse sind, die MES-FETs, bipolare Transistoren oder modulations-dotierte FETs umfaßt.
 11. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die zusammengesetzten Halbleiteranordnungen optoelektronische Anordnungen der Klasse sind, die LED, Laser und Lichtdetektoren umfassen.
 12. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die zusammengesetzten Halbleiteranordnungen Teil eines Schaltkreises sind, der aus Transistoren und optoelektronischen Anordnungen besteht.
 13. Verfahren nach einem beliebigen vorhergehenden Anspruch, dadurch gekennzeichnet, daß die ohmschen Kontakte für die Si-Anordnungen und zusammengesetzten Halbleiteranordnungen gebildet werden, nachdem die zusammengesetzte Halbleiter-Anordnung gebildet ist, und die ohmschen Kontakte für die Si-Anordnungen durch in der Schutzschicht hergestellte Öffnungen gebildet werden.

Revendications

1. Procédé de fabrication de dispositifs semi-conducteurs composites (210) en matériaux III-V ou II-VI et des dispositifs semi-conducteurs (200) en silicium sur un substrat commun d'un premier type de conductivité avec des interconnexions de faible résistance entre les dispositifs semi-conducteurs composites et les dispositifs en silicium formés dans le substrat, comprenant les étapes de:
 - (a) former des dispositifs si (200) ayant des régions d'un second type de conductivité opposée audit premier type de conductivité (34'/30'/32') et dans lesquels une des ré-

- gions (32') s'étend latéralement le long de la surface plane du substrat;
- (b) former une couche protectrice (16'/17') par dessus les dispositifs Si et le restant de ladite surface du substrat;
- (c) former des trous déplacés latéralement par rapport aux dispositifs Si à travers ladite couche protectrice pour exposer des régions de la surface dudit substrat, une partie du périmètre d'un desdits trous s'étendant dans la même région que ladite région étendue, la région du substrat sous ledit trou étant fortement doppée pour fournir une région de faible résistance (50) dudit second type de conductivité s'étendant vers la surface plane du substrat en contact avec ladite région étendue;
- (d) former une couche (54) dudit semi-conducteur composite sur la couche de protectrice et les régions exposées de ladite surface, ladite couche étant monocristalline au-dessus des régions exposées de la surface et polycristalline ailleurs;
- (e) enlever la couche polycristalline du semi-conducteur composite;
- (f) former lesdits dispositifs semi-conducteurs composites (56/58/60/62) ayant des jonctions formées de régions dudit second type de conductivité sur le semi-conducteur composite (54) monocristallin restant avec la région de faible résistance (50) en contact avec ladite région étendue (32) desdits dispositifs Si pour former des interconnexions de faible résistance dans ledit substrat; et
- (g) former des contacts ohmiques (72,70,28') sur lesdits dispositifs (200,210).
2. Procédé selon la revendication 1, caractérisé en ce que la région (50) de faible résistance est formée avant la formation de la couche protectrice (16'/17').
 3. Procédé selon la revendication 1, caractérisé en ce que la région de faible résistance est formée pendant la formation de la couche semi-conductrice composite.
 4. Procédé selon une revendication précédente quelconque, caractérisé en ce que le substrat est un monocristal: un substrat en silicium, ou un substrat en silicium sur saphire, ou un substrat en silicium sur isolant.
 5. Procédé selon une revendication précédente quelconque, caractérisé en ce que la couche protectrice est une couche de SiO_2 (16').
 6. Procédé selon une revendication précédente quelconque, caractérisé en ce que la couche protectrice comprend des couches de SiO_2 - (16') et Si_3N_4 (170).
 7. Procédé selon une revendication précédente quelconque, caractérisé en ce que le semi-conducteur composite est GaAs ou un alliage de GaAs.
 8. Procédé selon la revendication 7, caractérisé en ce que le dispositif semi-conducteur en arseniure de gallium est un dispositif optoélectronique (210).
 9. Procédé selon une revendication précédente quelconque, caractérisé en ce que les dispositifs Si font partie d'un circuit Si.
 10. Procédé selon une revendication précédente quelconque, caractérisé en ce que les dispositifs semi-conducteurs composites sont des transistors de la classe comprenant les transistors à effet de champ MESFET, les transistors bipolaires et les transistors à effet de champ doppés par modulation.
 11. Procédé selon une revendication précédente quelconque, caractérisé en ce que les dispositifs semi-conducteurs composites sont des dispositifs optoélectroniques de la classe comprenant les diodes à luminescence, les lasers et les détecteurs de lumière.
 12. Procédé selon une revendication précédente quelconque, caractérisé en ce que les dispositifs semi-conducteurs composites font partie d'un circuit formé de transistors et de dispositifs optoélectronique.
 13. Procédé selon une revendication précédente quelconque, caractérisé en ce que les contacts ohmiques pour lesdits dispositifs Si et lesdits dispositifs semi-conducteurs composites sont formés après que le dispositif semi-conducteur composite a été formé et les contacts ohmiques pour les dispositifs Si sont formés à travers des trous aménagés dans ladite couche protectrice.

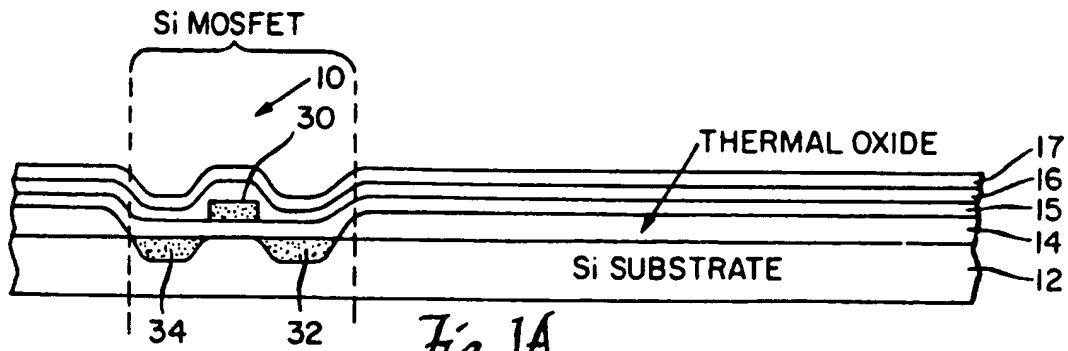


Fig. 1A

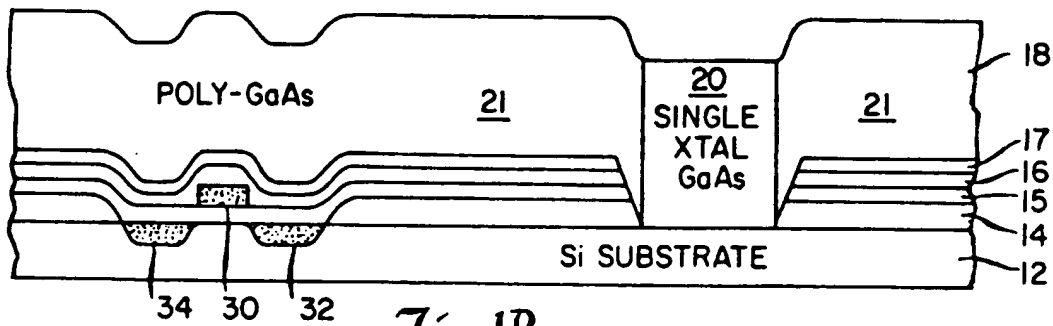


Fig. 1B

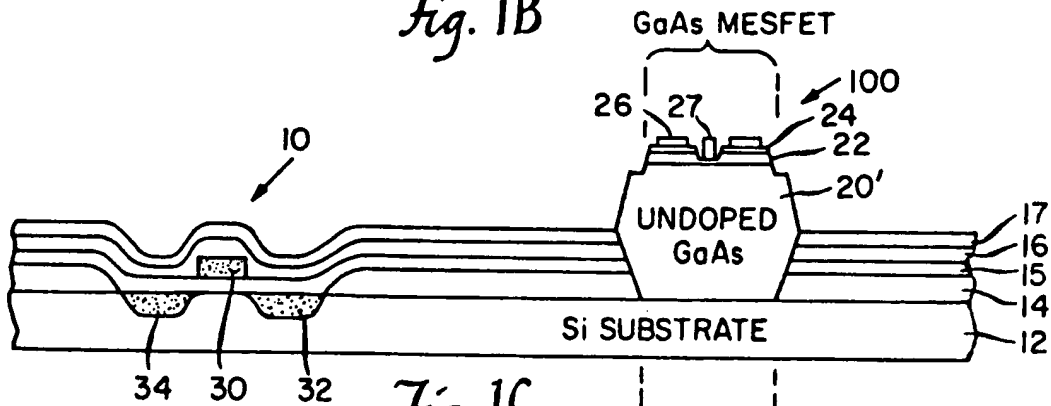


Fig. 1C

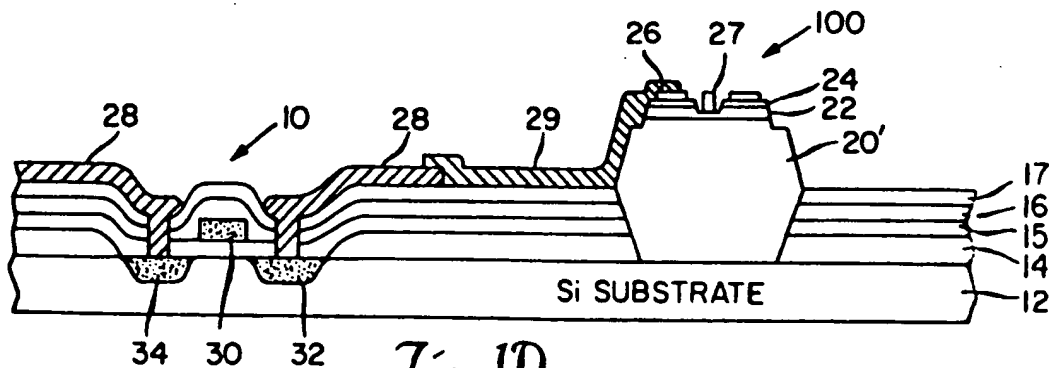


Fig. 1D

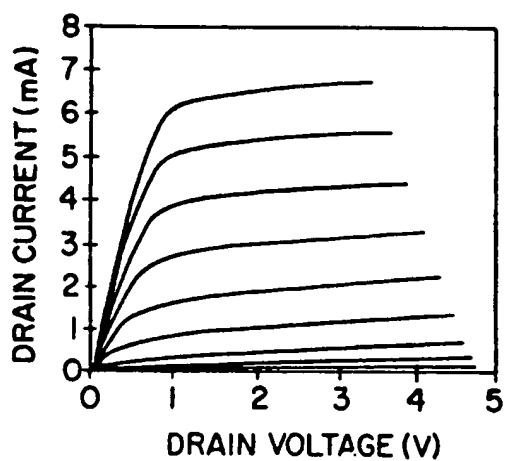


Fig. 2

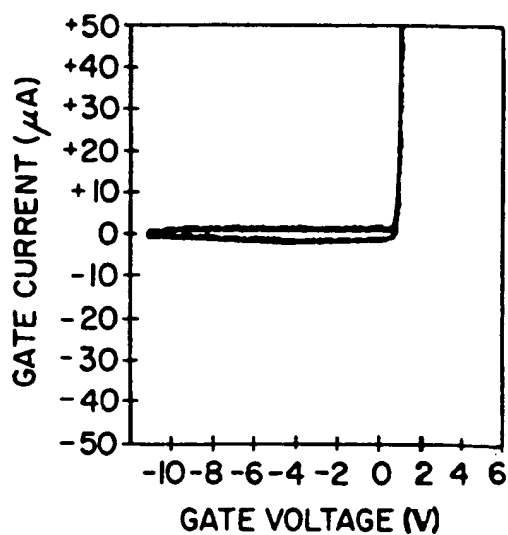


Fig. 3

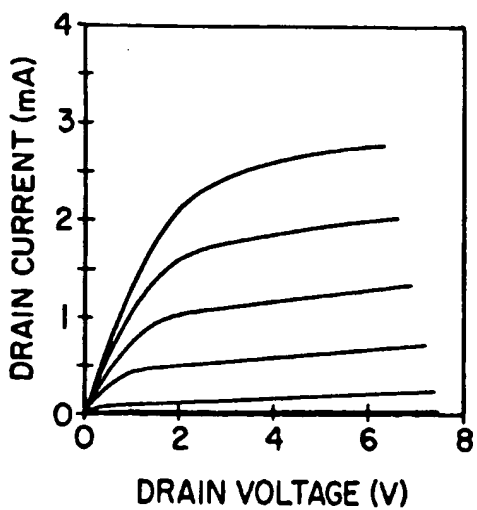


Fig. 4A

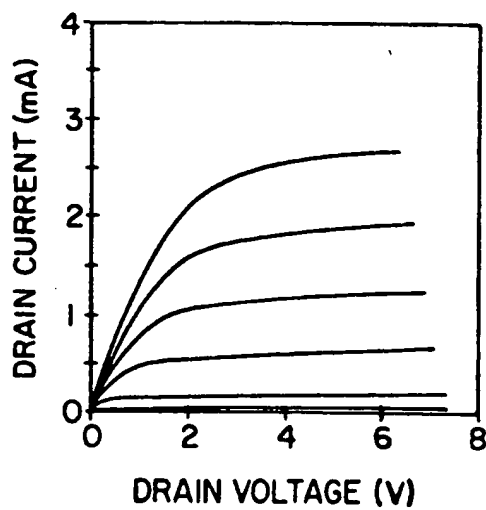


Fig. 4B

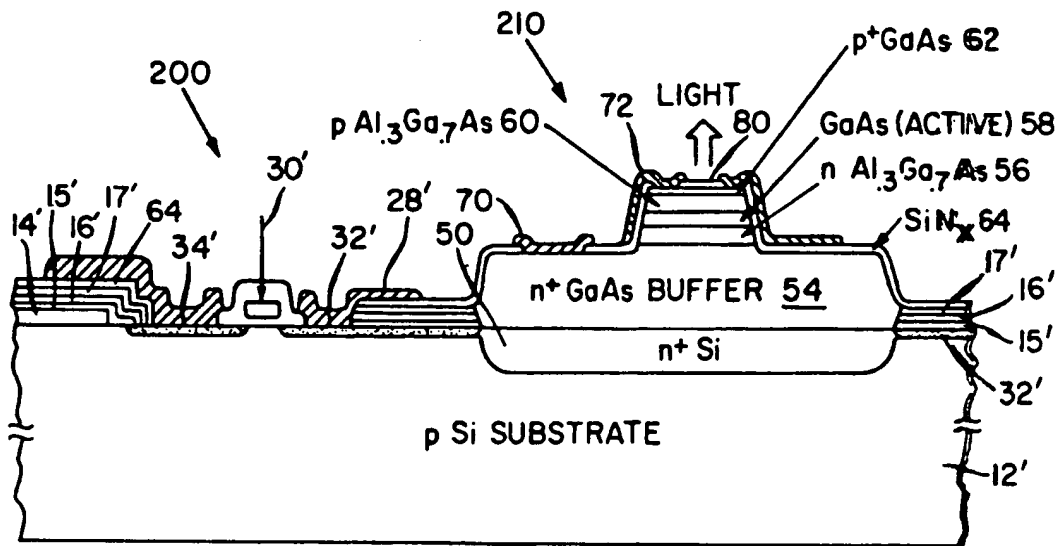


Fig. 5

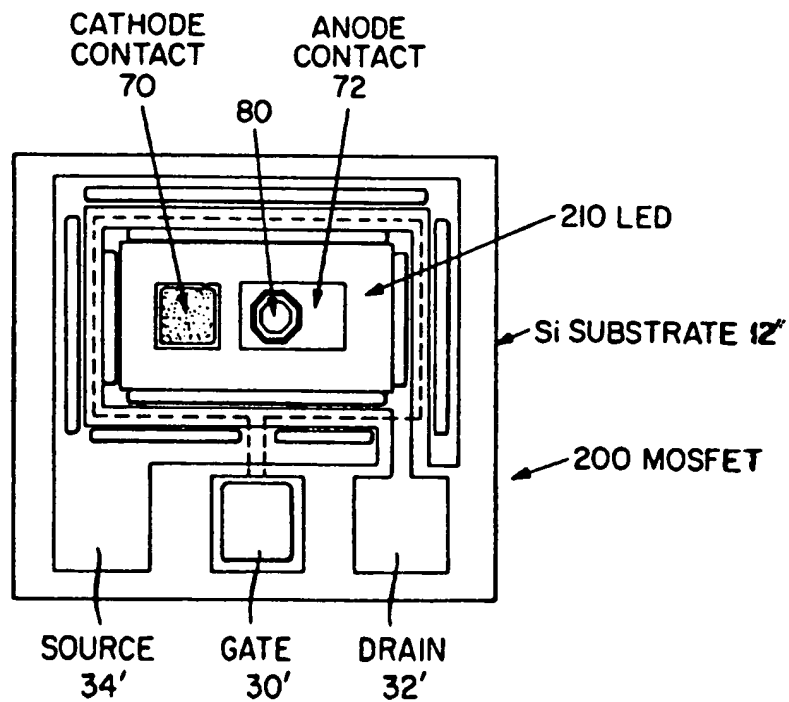
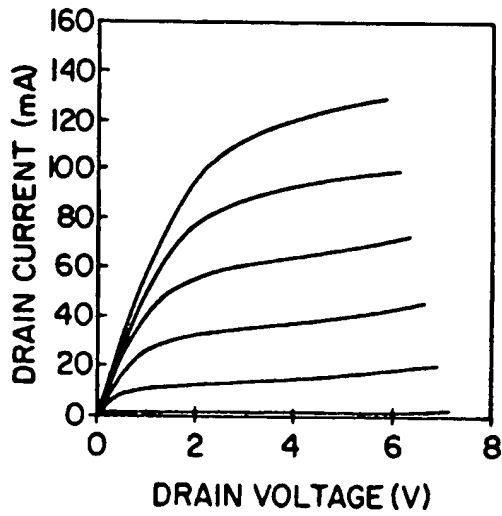
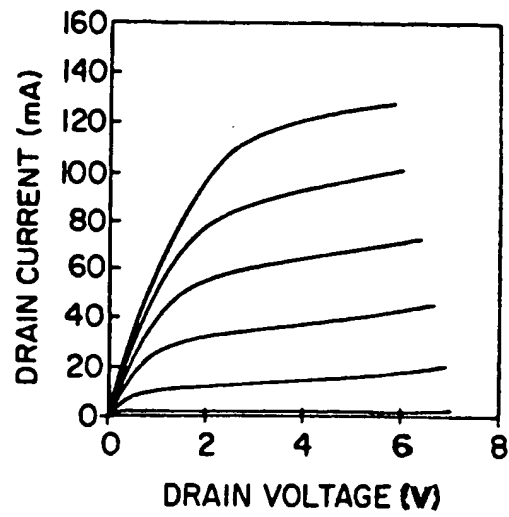
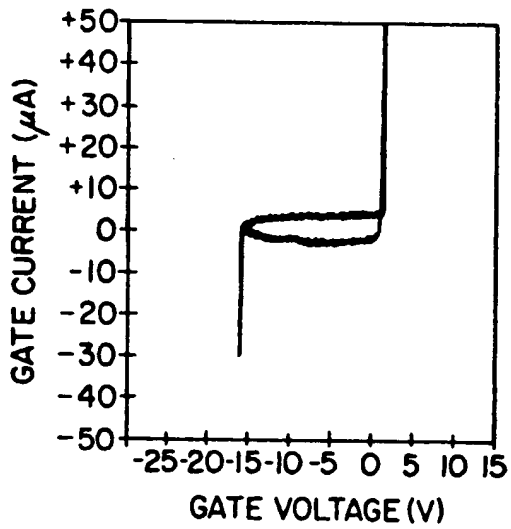
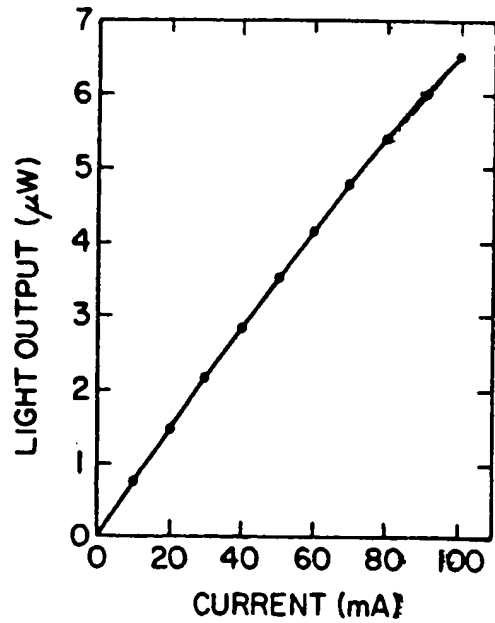
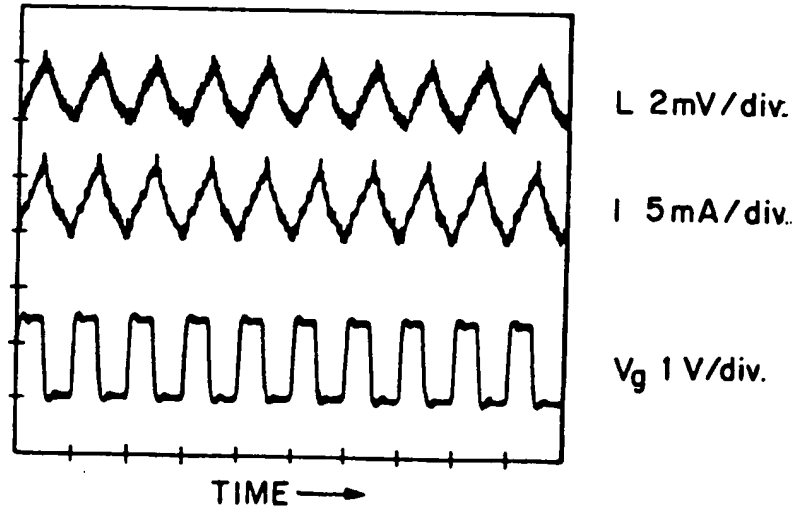
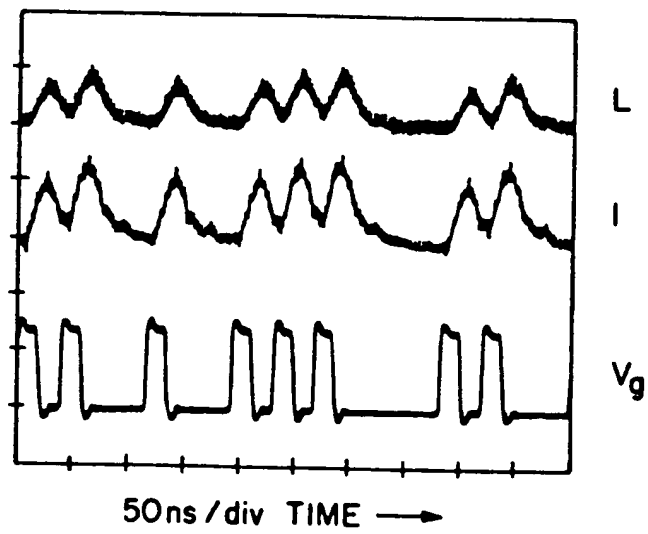


Fig. 6

*Fig. 7A**Fig. 7B**Fig. 8**Fig. 9*

*Fig. 10A**Fig. 10B*

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.